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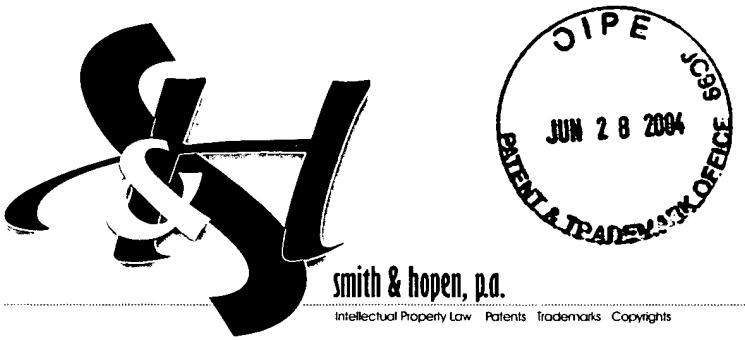

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Intellectual Property Law Patents Trademarks Copyrights

June 25, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants: Praveen K. Samudrala **Examiner: Unassigned**
Serial No.: 10/708,268 **Art Unit: 2816**
Filing Date: 02/20/2004
For: Method and Apparatus for Creating Circuit Redundancy in Programmable Logic Devices
Our Reference No.: 1372.136.PRC

Dear Sir:

Enclosed please find the following:

1. Information Disclosure Statement By Applicants- 2 pages;
2. Copies of two (2) U.S. Patent Documents;
3. Copies of the front covers of nine (9) Non-Patent Literature Documents; and
4. Self-addressed, postage prepaid post card to serve as a receipt for items 1-3.

Very respectfully,

SMITH & HOPEN

Molly L. Sauter

By: Molly L. Sauter
molly.sauter@smithhopen.com

MLS/cm
enclosure

CERTIFICATE OF MAILING
(37 C.F.R. 1.8)

I HEREBY CERTIFY that this correspondence is being mailed with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 25, 2004.

Date: **June 25, 2004**

Charlene Morgan

Attorney-Client Privileged Communication

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	2816
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,298,289	10/02/2001	Lloyd et al.	
	2	US- 4,964,126	10/16/1990	Musicus et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

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Sheet 2 of 2

Complete if Known	
Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	2816
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	EDUARDO AUGUSTO BEZERRA ET AL., Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques: A Case Study.	
	2	ZOLTAN MEGGYESI ET AL., FPGA Design in the Presence of Single Event Upsets, CERN, Geneva, Switerland.	
	3	Single Event Upset (SEU) Mitigation by Virtual Triple Modular Redundancy (TMR) in Design Reduces Manufacturing Cost and Lowers Power, Alternative System Concepts, Inc., pg 1-7	
	4	EARL FULLER ET AL., Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing, pg. 1-11.	
	5	K. NIKOLIC ET AL., Fault-Tolerant Techniques for Nanocomputers, TNT2001, Sept. 3-7, 2001, Segovia, Spain.	
	6	CARL CARMICHEAL ET AL., SEU MitigationTechniques for Virtex FPGAs in Space Application.	
	7	PRAVEEN SAMUDRALA ET AL., Single Event Upsets and Mitigation Technigues: A Survey, pages 1-15.	
	8	SRINIVAS KATKOORI, SEU Tolerant Design Techniques for Space Based RC Implementations, IR & D Project, March 28, 2001.	
	9	PRAVEEN K. SAMUDRALA, Synthesis of SEU Tolerant FPGAs, January 22, 2003, pages 1-53.	

Examiner Signature		Date Considered	

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